Further, the drain region 814 of the switching TFT 8201 is connected to the gate electrode 830 of the EL driver TFT 8202. Although not shown in the figure, specifically the gate electrode 830 of the EL driver TFT 8202 is electrically connected to the drain region 814 of the switching TFT 8201 through the drain wiring (also referred to as a connection wiring) 822. The source wiring 831 of the first EL driver TFT 8202 is connected to an power source supply line (not shown in the figure).

The first EL driver TFT 8202 is an element for controlling the amount of electric current injected to the EL element, and a relatively large amount of current flows. It is therefore preferable to design the channel width W to be larger than the channel width of the switching TFT. Further, it is preferable to design the channel length L such that an excess of electric current does not flow in the EL driver TFT 8202. It is preferable to have from 0.5 to 2 μA (more preferably between 1 and 1.5 μA) per pixel.

In addition, by making the film thickness of the active layers (particularly the channel forming region) of the EL driver TFT 8202 thicker (preferably from 50 to 100 nm, even better between 60 and 80 nm), deterioration of the TFT may be suppressed. Conversely, it is also effective to make the film thickness of the active layer (particularly the channel forming region) thinner (preferably from 20 to 50 nm, even better between 25 and 40 nm), from the standpoint of making the off current smaller, for the case of the switching TFT 8201.

The structures of the TFTs formed within the pixel are explained above, but a driver circuit is also formed simultaneously at this point. A CMOS circuit. which becomes a basic unit for forming the driver circuit. is shown in Fig. 18.

A TFT having a structure in which hot carrier injection is reduced without an excessive drop in the operating speed is used as an n-channel TFT 8204 of the CMOS circuit in Fig. 18. Note that the term driver circuit indicates a source signal line driver circuit and

a gate signal line driver circuit here. It is also possible to form other logic circuit (such as a level shifter, an A/D converter, and a signal division circuit).

An active layer of the n-channel TFT 8204 of the CMOS circuit contains a source region 835, a drain region 836, an LDD region 837, and a channel forming region 862. The LDD region 837 overlaps with a gate electrode 839 through the gate insulating film 818. Therefore, the LDD region 837 is made to overlap with the gate electrode completely. It is preferable to reduce the resistance component as much as possible. The reference numeral 838 is a mask to form the channel formation region.

Formation of the LDD region 837 on only the drain region 836 side is so as not to have drop the operating speed. Further, it is not necessary to be very concerned about the off current with the n-channel TFT 8204, and it is good to place more importance on the operating speed. Thus, it is desirable that the LDD region 837 is made to completely overlap the gate electrode to decrease a resistance component to a minimum. It is therefore preferable to eliminate so-called offset.

Furthermore, there is almost no need to be concerned with degradation of a p-channel TFT 8205 of the CMOS circuit, due to hot carrier injection, and therefore no LDD region need be formed in particular. Its active layer therefore contains a source region 840, a drain region 841, and a channel forming region 861, and a gate insulating film 818 and a gate electrode 843 are formed on the active layer. It is also possible, of course, to take measures against hot carrier injection by forming an LDD region similar to that of the n-channel TFT 8204. The reference numeral 842 is a mask to form the channel formation region.

Further, the n-channel TFT 8204 and the p-channel TFT 8205 have source wirings 844 and 845, respectively, on their source regions, through the first interlayer insulating

film 820. In addition, the drain regions of the n-channel TFT 8204 and the p-channel TFT 8205 are mutually connected electrically by a drain wiring 846.

Next, reference numeral 847 denotes a first passivation film, and its film thickness may be set from 10 nm to 1 μm (preferably between 200 and 500 nm). An insulating film containing silicon (in particular, it is preferable to use an oxidized silicon nitride film or a silicon nitride film) can be used as the passivation film material. The passivation film 847 possesses a role of protecting the TFTs from alkaline metals and moisture. Alkaline metals such as sodium are contained in an EL layer formed last on the final TFT (in particular, the EL driver TFT). In other words, the first passivation film 847 works as a protecting layer so that these alkaline metals (mobile ions) do not penetrate into the TFT.

Further, reference numeral 848 denotes a second interlayer insulating film, which has a function as a leveling film for performing leveling of a step due to the TFTs. An organic resin film is preferable as the second interlayer insulating film 848, and one such as polyimide, polyamide, acrylic, or BCB (benzocyclobutene) may be used. These organic resin films have the advantages of easily forming a good, level surface, having a low specific dielectric constant. The EL layer is extremely sensitive to unevenness, and therefore it is preferable to mostly absorb the TFT step by the second interlayer insulating film 848. In addition, it is preferable to form the low specific dielectric constant material thickly in order to reduce the parasitic capacitance formed between the gate signal wiring, the data signal wiring and the cathode of the EL element. The thickness, therefore, is preferably from 0.5 to 5 μm (more preferably between 1.5 and 2.5 μm).

Further, reference numeral 849 denotes a pixel electrode (EL element anode) made from a transparent conducting film. After forming a contact hole (opening) in the second interlayer insulating film 848 and in the first passivation film 847, the pixel electrode 849 is formed so as to be connected to the drain wiring 832 of the first EL driver TFT 8202. Note